PATENT ABSTRACTS OF JAPAN

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(54) COMPUTER SYSTEM

(57)Abstract:
PURPOSE: To increase the memory access speed by simplifying the decoder condition for determination of a RAG line to be energized.
CONSTITUTION: A RAS0 line and a RAS1 line are connected to two 2M-byte banks constituting a system memory 13, and a RAS2 line is connected to one 8M-byte bank constituting an extended memory 41, and a RAS4 line and a RAS5 line are connected to two 4M-byte banks constituting an extended memory 42. These banks are rearranged in a DRAM logical address space in the order of memory size so that a lower address range is assigned to the bank having a larger memory size. In this memory arrangement, a bit string always exists which has a value common to all memory address values belonging to the address range assigned to each of DRAM banks. These common bit strings are used as decode conditions of corresponding RAS lines.